Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) An apparatus comprising:

a signal layer including a first and a second signal trace located along a first plane, each of the first and second signal traces comprises a first segment with a first segment width, and a second segment with a second segment width;

a ~~first~~ reference layer~~plane~~ located along a second plane that is substantially parallel with the first plane coupled to the first and the second signal trace, the reference layer includes~~ing~~ a ~~first~~ slot substantially parallel to the first and second signal traces, the slot comprising a first portion and a second portion having a first portion width and a second portion width, respectively; and

~~a dielectric layer having at least a first portion disposed between the signal layer and the first reference plane~~

wherein the first and second portions of the slot correspond to the first and second segments, respectively, of the first and second signal traces.

2. (Currently amended) The apparatus of claim 1, further comprising a dielectric layer that is at least partially disposed between the signal layer and the reference layer ~~wherein each of the first and second signal traces comprise a first portion with a first width, and a second portion with a second width~~.

3. (Currently amended) The apparatus of claim ~~2~~ 1 wherein spacing between the first and the second signal trace remains substantially constant in both the first and second segments~~the first slot comprises a first portion and a second portion having a first slot width and a second slot width, respectively~~.

4. (Cancelled)

5. (Currently amended) The apparatus of claim 1,~~3~~ wherein each of the first and second signal traces further comprises a third segment~~portion~~ with a third segment width and the ~~first~~ slot comprises a third portion, comprising a third ~~slot~~ portion width, corresponding to the third segment~~portion~~ of the first and second signal traces.

6. (Currently amended) The apparatus of claim 1 wherein the first and second signal traces have a first and a second signal trace width respectively, wherein the first signal trace width is substantially the same as the second signal trace width.

7. (Currently amended) The apparatus of claim 1 wherein the signal layer further includes a third and a fourth pair of signal traces and another ~~second~~ slot.

8. (Currently amended) The apparatus of claim 2~~1~~ further comprising:

another ~~second~~ reference ~~plane~~layer located along a third plane that is substantially parallel with the first plane, coupled to the first and the second signal trace, the other reference layer including another ~~second~~ slot substantially parallel to the first and second signal traces; and

the dielectric layer is further ~~includes a second portion~~ partially disposed between the signal layer and the other ~~second~~ reference layer~~plane~~.

9. (Withdrawn) An assembly comprising:

an apparatus comprising:

a signal layer including a first and second signal trace;

a first reference plane including a first slot substantially parallel to the first and second signal traces; and

a dielectric layer having at least a first portion disposed between the signal layer and the first reference plane;

a processor coupled to the apparatus; and

a networking interface coupled to the apparatus.

10. (Withdrawn) The assembly of claim 9 wherein the first and second signal traces are coupled to the processor and the memory device.

11. (Withdrawn) The assembly of claim 9 wherein each of the first and second signal traces comprise a first portion with a first width and a second portion with a second width.

12. (Withdrawn) The assembly of claim 11 wherein the first slot comprises a first portion and a second portion having a first slot width and a second slot width, respectively.

13. (Withdrawn) The assembly of claim 12 wherein the first and second portions of the first slot correspond to the first and second portions, respectively, of the first and second signal traces.

14. (Withdrawn) The assembly of claim 9 further comprising:

a second reference plane including a second slot substantially parallel to the first and second signal traces; and

the dielectric layer further includes a second portion disposed between the signal layer and the second reference plane.

15. (Withdrawn) The assembly of claim 9 wherein the first and second signal trace are to facilitate propagation of a differential signal pair.

16. (Withdrawn) A system comprising:

an assembly comprising:

an apparatus comprising:

a signal layer including a first and second signal trace;

a first reference plane including a first slot substantially parallel to the first and second signal traces; and

a dielectric layer having at least a first portion disposed between the signal layer and the first reference plane; and

a processor coupled to the apparatus; and

a networking device coupled to the assembly.

17. (Withdrawn) The system of claim 16 wherein the a assembly further comprises a networking interface, wherein the networking interface is coupled to the networking device.

18. (Withdrawn) The system of claim 16 wherein the assembly further comprises an interface to persistent storage and wherein the system further comprises persistent storage coupled to the interface to persistent storage.

19. (Withdrawn) A method of routing circuit board traces comprising:

routing a first signal trace and a second signal trace substantially parallel to the first signal trace on a signal plane of a circuit board; and

routing a slot in a reference plane of the circuit board substantially parallel to the first second signal traces, for at least a portion of the first and second signal traces.

20. (Withdrawn) The method of claim 19 wherein the substantially parallel portion of the first and second signal traces comprises a first portion with a first width and a second portion with a second width.

21. (Withdrawn) The method of claim 20 wherein said routing of a slot comprises routing a first portion and a second portion of the slot, with a first and a second slot width respectively, corresponding to the first and second portions of the first and second signal traces.